Introduction

- 1964
  - Fairchild 发明第一個線性 IC：OP μA702
  - Operational amplifier is an analog block can perform mathematical operations like:
    - Addition, subtraction, multiplication, integration, differentiation
    - Comparators, waveform generators, current sources, voltage regulator, filters, and other signal processing functions
Outline

2.1 The Ideal Op Amp (理想運算放大器)
2.2 The Inverting Configuration (反相組態)
2.3 The Non-inverting Configuration (非反相組態)
2.4 Differential amplifier (差動放大器)
2.5 Effect of Finite Open-Loop Gain and Bandwidth on Circuit Performance (有限開迴路增益與頻寬對電路性能的影響)
2.6 Large-Signal Operation of Op Amps (運算放大器的大信號操作)
2.7 DC Imperfections (直流非理想特性)
2.8 Integrator and Differentiator (積分器與微分器)

Figure 2.1 Circuit symbol for the op amp.

Figure 2.2 The op amp shown connected to dc power supplies.
理想 Op Amp 的等效電路

The input-output relationship is

\[ v_O = A(v_2 - v_1) \]

- \( v_2 \) is the positive or noninverting input
- \( v_1 \) is the negative or inverting input
- \( A \) is the differential gain (open-loop gain)
- \( v_O \) is the output voltage
- \( v_2 - v_1 \) denotes the differential input

Figure 2.3 Equivalent circuit of the ideal op amp.

Ideal Op Amp Circuits

- OP amp 为直流放大器
- An op amp can be represented to first order by a voltage-controlled voltage source.
- An ideal op amp is
  - Zero input current (infinite input impedance)
  - Zero output impedance
  - Zero common mode gain (infinite CMRR)
  - Infinite gain
  - Infinite bandwidth
Differential Mode and Common Mode

- The differential mode input
  \[ v_{id} = v_2 - v_1 \]
- The average or common mode input
  \[ v_{icm} = \frac{v_2 + v_1}{2} \]
  \[ v_1 = v_{icm} - \frac{v_{id}}{2} \]
  \[ v_2 = v_{icm} + \frac{v_{id}}{2} \]

Figure 2.4 Representation of the signal sources \( v_1 \) and \( v_2 \) in terms of their differential and common-mode components.

Outline 大綱

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2.4 Differential amplifier（差動放大器）
2.5 Effect of Finite Open-Loop Gain and Bandwidth on Circuit Performance（有限開迴路增益與頻寬對電路特性的影響）
2.6 Large-Signal Operation of Op Amps（運算放大器的大信號操作）
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### Inverting Configuration

- An inverting amplifier uses negative feedback.
- Virtual short $\rightarrow$ virtual ground ($v_1 = 0$)

$$v_2 - v_1 = \frac{v_2}{A} = 0 \implies v_2 = v_1$$

![Figure 2.5 The inverting closed-loop configuration.](image)

### Closed-loop Gain

- The inverting amplifier has
  - A low output impedance (ideally zero)
  - A voltage gain set by a resistor ratio
  - A relatively low input impedance ($\approx R1$)
  - The output is inverted

$$G = \frac{v_o}{v_i} = \frac{R_o}{R_i}$$

![Figure 2.6 Analysis of the inverting configuration. The circled numbers indicate the order of the analysis steps.](image)
Finite Open-loop Gain

- Effect of finite gain on inverting amp

\[
i_i = \frac{v_i + v_o}{R_v}
\]

\[
v_o = -\frac{v_o}{A} - i_i R_2 = -\frac{v_o}{A} \left( \frac{v_i + v_o}{R_1} \right) R_2
\]

\[G = \frac{v_o}{v_i} = \frac{-R_2 / R_v}{1 + (1 + R_2 / R_v) / A}
\]

- If \( A \to \infty \), the closed-loop gain reduces to

\[G = \frac{v_o}{v_i} = \frac{-R_2}{R_v}
\]

Figure 2.7 Analysis of the inverting configuration taking into account the finite open-loop gain of the op amp.

Input and Output Resistance

- 閉迴路反相放大器的輸入電阻

\[R_1 \equiv \frac{v_i}{i_i} = \frac{v_i}{v_j} = R_i
\]

- 要得到較高的輸入電阻值，則必須選定數值大的 \( R_1 \)，同時要得到較高的增益 \( R_2 / R_1 \)，則 \( R_2 \) 的值可能大到不切實際。

- Ex: \( R_1 = 1M \Omega \), \( G = -100 \), \( R_2 = 100M \Omega \)!

- 閉迴路反相放大器的輸出電阻為0
Example 2.2 (T-network)

Figure 2.8 Circuit for Example 2.2. The circled numbers indicate the sequence of the steps in the analysis.

\[ R_1 = 1 \text{M} \Omega \cdot R_2 = 1 \text{M} \Omega \cdot G = -100 \rightarrow R_3 = 1 \text{M} \Omega \cdot R_3 = 10.2 \text{k} \Omega! \]

Figure 2.9 A current amplifier based on the circuit of Fig. 2.8. The amplifier delivers its output current to \( R_4 \). It has a current gain of \((1 + R_2/R_3)\), a zero input resistance, and an infinite output resistance. The load \( (R_4) \), however, must be floating (i.e., neither of its two terminals can be connected to ground).

Weighted Summer 加權加總器

- Summing amplifier can be break into 2 separate operations
  - \( R_1 \) converts the input voltage into a current \( i_{R1} \)
  - This current is then the input to a transresistance amplifier formed by the op and \( R_2 \)

\[ I = I_1 + I_2 + \cdots + I_n = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \cdots + \frac{V_n}{R_n} \]

\[ V_0 = -(R_1) = \left( \frac{R_1}{V_1} + \frac{R_2}{V_2} + \cdots + \frac{R_n}{V_n} \right) \]

Figure 2.10 A weighted summer.
Weighted Summer

\[ v_O = v_1 \left( \frac{R_2}{R_4} \right) \left( \frac{R_e}{R_b} \right) + v_2 \left( \frac{R_a}{R_2} \right) \left( \frac{R_e}{R_b} \right) - \frac{v_3}{R_3} - v_4 \left( \frac{R_i}{R_4} \right) \]

*Figure 2.11* A weighted summer capable of implementing summing coefficients of both signs.

Outline 大綱

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2.6 Large-Signal Operation of Op Amps（運算放大器的大信號操作）
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The Non-inverting Configuration

- A noninverting amplifier is a closed loop amplifier provides negative feedback, $R_1$ and $R_2$ comprise the feedback network.
- The op amp has a virtual short circuit.

![Figure 2.12 The noninverting configuration.](image)

\[ v_i = v_2 \]
\[ v_o = \frac{R_1}{R_1 + R_2} v_o \]
\[ G = \frac{v_o}{v_i} = 1 + \frac{R_2}{R_1} \]

Degenerative Feedback

- An ideal op amp will have a virtual short circuit between its input terminals as long as it has a negative feedback connection.
- A non-inverting amplifier is a closed loop amplifier provides negative or degenerative feedback, $R_1$ and $R_2$ comprise the feedback network.
- The noninverting amplifier has
  - A very high input impedance (ideally infinite)
  - A low output impedance (ideally zero)
  - A well-controlled voltage gain set by a resistor ratio
Finite Open-loop Gain

- Effect of finite gain on non-inverting amp

\[
G = \frac{v_O}{v_i} = \frac{1 + \frac{R_2}{R_1}}{1 + \left(1 + \frac{R_2}{R_1}\right)/A}
\]

- If \( A \to \infty \), the closed-loop gain reduces to

\[
G = \frac{v_O}{v_i} = 1 + \frac{R_2}{R_1}
\]

Voltage Follower

- The Unity-Gain Amplifier
  - also called voltage follower or unity-gain follower
  - is a special case of the noninverting amplifier
    \( R_1 = \infty, \ R_2 = 0 \)  
    \( v_O = v_I \)

Figure 2.14 (a) The unity-gain buffer or follower amplifier, (b) Its equivalent circuit model.
The Differential Amplifier

\[ v_O = A_d v_{dd} + A_{cm} v_{cm} \]

- The ratio of the differential mode gain, \( A_d \), to the common mode gain, \( A_{cm} \), is called the common mode rejection ratio (CMRR).

\[ CMRR_{dB} = 20 \log \left( \frac{A_d}{A_{cm}} \right) = A_d (v_{dd}) - A_{cm} (v_{cm}) \]

- The CMRR should be as large as possible.

Figure 2.15 Representing the input signals to a differential amplifier in terms of their differential and common-mode components.
Differential Amplifier

Let the non-inverting gain equal the inverting gain

\[
\left( \frac{R_3}{R_1 + R_3} \right) \left( 1 + \frac{R_2}{R_1} \right) = -\frac{R_2}{R_1}
\]

\[
\frac{R_4}{R_1 + R_4} = \frac{R_4}{R_1 + R_4}
\]

\[
\frac{R_s}{R_s} = \frac{R_2}{R_1}
\]

\[
v_o = \frac{R_2}{R_1} (v_{t2} - v_{t1})
\]

Figure 2.16 A difference amplifier.

By Superposition

By superposition

\[
v_{oi} = \frac{R_1}{R_t} v_{t1}
\]

\[
v_{oi} = \left( \frac{R_1}{R_1 + R_4} \right) \left( 1 + \frac{R_2}{R_1} \right) v_{t1}
\]

\[
v_o = v_{oi} + v_{oi} = -\frac{R_2}{R_1} v_{t1} + \left( \frac{R_4}{R_1 + R_4} \right) \left( 1 + \frac{R_2}{R_1} \right) v_{t2}
\]

Let \( R_3 = R_1 \) and \( R_4 = R_2 \)

\[
v_o = \frac{R_2}{R_1} (v_{t2} - v_{t1}) = A_v v_{id}
\]

Figure 2.17 Application of superposition to the analysis of the circuit of Fig. 2.16.
共模信號分析

\[ i_1 = \frac{1}{R_1} \left( v_{cm} - \frac{R_1}{R_1 + R_2} v_{os} \right) = v_{os} \frac{R_1}{R_1 + R_2} = i_1 \]

\[ v_o = \frac{R_4}{R_1 + R_4} v_{os} - i_2 R_3 \]

\[ = \frac{R_1}{R_1 + R_4} v_{os} - \left( \frac{R_1}{R_1 + R_4} \frac{R_3}{R_1} \right) v_{os} \]

\[ = R_1 \left( 1 - \frac{R_3}{R_1} \frac{R_1}{R_1 + R_4} \right) v_{os} \]

\[ A_{cm} = \frac{v_o}{v_{os}} = \frac{R_4}{R_1 + R_4} \left( 1 - \frac{R_3}{R_1} \frac{R_1}{R_1 + R_4} \right) \]

Let \( R_3 = R_1 \) and \( R_4 = R_2 \)

\[ \rightarrow A_{cm} = 0 \]

Differential Input Resistance

If \( R_3 = R_1 \) and \( R_4 = R_2 \)

\[ v_{id} = i_1 R_1 + 0 + i_1 R_1 \]

\[ R_{id} = 2R_1 \]
The Instrumentation Amplifier

1. Instrumentation amplifier = 2 noninverting amplifiers + differential amplifier

\[ A_o = \frac{V_o}{V_i} = \left(1 + \frac{R_2}{R_1}\right) \frac{R_2}{R_1} \]

- 輸入共模信號在第一級會被放大
- 第一級兩個放大器要完全匹配，否則錯誤信號在第二級會被放大
- 改變差模增益時，必須同時改變R1

**Figure 2.20** A popular circuit for an instrumentation amplifier: (a) Initial approach to the circuit; (b) The circuit in (a) with the connection between node X and ground removed and the two resistors R1 and R2 lumped together. This simple wiring change dramatically improves performance; (c) Analysis of the circuit in (b) assuming ideal op amps.

Analysis of Instrumentation Amplifier

\[ I_{2R} = \frac{V_{o2}}{2R_1} \]
\[ V_{o2} - V_{o1} = \left(1 + \frac{2R_2}{R_1}\right) V_{o1} \]
\[ V_o = \frac{R_4}{R_3} \left(V_{o2} - V_{o1}\right) = \frac{R_4}{R_3} \left(1 + \frac{R_2}{R_1}\right) V_{o2} \]

\[ A_o = \frac{V_{o2}}{V_{o1}} = \left(1 + \frac{R_2}{R_1}\right) \frac{R_2}{R_1} \]
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Figure 2.22 Open-loop gain of a typical general-purpose internally compensated op amp.
Finite Bandwidth

- Internally compensated Op Amps can be modeled as having a single pole low pass transfer function
  \[ A(s) = \frac{A_0}{1 + \frac{s \omega_b}{\mu}} \]

- For frequencies well above \( \omega_b \), \[ |A(j\omega)| = \frac{A_0 \omega_b}{\omega} \approx \text{GBW} \]

- The product of the frequency and the magnitude of the transfer function is a constant called the gain-bandwidth product (GBW) on the high frequency asymptote.
  \[ \omega |A(j\omega)| = A_0 \omega_b = \omega_b = \text{GBW} \]

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Output Voltage Saturation
Output Current Limits

Figure 2.25 (a) A noninverting amplifier with a nominal gain of 10 V/V designed using an op amp that saturates at ±13-V output voltage and has ±20-mA output current limits. (b) When the input sine wave has a peak of 1.5 V, the output is clipped off at ±13 V (rated output voltage).

Slew Rate 迴轉率

Figure 2.26 (a) Unity-gain follower. (b) Input step waveform. (c) Linearly rising output waveform obtained when the amplifier is slew-rate limited. (d) Exponentially rising output waveform obtained when $V$ is sufficiently small so that the initial slope ($v_I$) is smaller than or equal to SR.
Full-Power Bandwidth

- Full-Power Bandwidth $f_M$

  - When the frequency $\omega$ is higher than $\omega_M$, the peak amplitude of the output sine wave is

  \[
  v_I = V \sin \omega t \\
  \frac{dv_I}{dt} = \omega V \cos \omega t \\
  \omega_O V_{\max} = SR \\
  f_M = \frac{SR}{2\pi V_{\max}}
  \]

  \[V_O = V_{\max} \left( \frac{\omega_M}{\omega} \right)\]

Figure 2.27 Effect of slew-rate limiting on output sinusoidal waveforms.

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2.7 DC Imperfections
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Input Offset Voltage

- The output voltage is not zero if the two inputs of Op Amp are tied together.
- The input offset voltage $V_{OS}$ is the voltage need to applied at the input to produce zero output voltage.
- Because the offset voltage is random, there isn’t any way of compensating for it. Same as input offset current.

Figure 2.28 Circuit model for an op amp with input offset voltage $V_{OS}$.

Ex 2.23

Figure E2.23 Transfer characteristic of an op amp with $V_{OS} = 5$ mV.

Figure 2.29 Evaluating the output dc offset voltage due to $V_{OS}$ in a closed-loop amplifier.
Offset Voltage Trimming

Figure 2.30 The output dc offset voltage of an op amp can be trimmed to zero by connecting a potentiometer to the two offset-nulling terminals. The wiper of the potentiometer is connected to the negative supply of the op amp.

Capacitively Coupled Amplifier

Figure 2.31 (a) A capacitively coupled inverting amplifier, and (b) the equivalent circuit for determining its dc output offset voltage $V_O$. 

$V_O = V_{ox}$
Input Bias and Offset Currents

- The input currents $I_{B1}$ and $I_{B2}$ due to input impedance of OP Amp is not infinite.
- The input bias current $I_B$ is defined as the average value of two bias currents.
- The difference between $I_{B1}$ and $I_{B2}$ is called the input offset current $I_{OS}$

![Figure 2.32](image)

The op-amp input bias currents represented by two current sources $I_{B1}$ and $I_{B2}$.

\[
I_B = \frac{I_{B1} + I_{B2}}{2}, \quad I_{OS} = |I_{B1} - I_{B2}|
\]

Effect of Input Bias Current

- Induce output offset voltage ($V_i=0$)

\[
V_O|_{I_{B1}=0} = I_B R_2 = I_B R_2
\]

![Figure 2.33](image)

Analysis of the closed-loop amplifier, taking into account the input bias currents.
Input Bias Current Compensation

- Add $R_i = R_i' / R_i$ at non-inverting node
  
  \[ V_O = -I_{B2}R_i + R_3(I_{B1} - I_{B2}R_i / R_i') \]

  - If $I_{B1} = I_{B2} = I_B$, then
    
    \[ V_O = I_B[R_2 - R_i(1 + R_i / R_i')] \]
  
  - $V_O = 0$, then
    
    \[ R_i = \frac{R_2}{R_i + R_2} = \frac{R_2R_i'}{R_i' + R_2} \]

  - If
    
    \[ I_{B1} = I_B + I_{0B} / 2, \quad I_{B2} = I_B - I_{0B} / 2 \]
    
    \[ V_O = I_{0B}R_2 \]

  \[ \text{Figure 2.34 Reducing the effect of the input bias currents by introducing a resistor } R_3. \]

AC-coupled Amplifier

- 要將輸入偏壓電流的效應減到最小，必須在正輸入端放一個與反相端看過去的電阻值相等的電阻。

- Op amp的輸入端與地之間必須提供連續的直流路徑。

  \[ \text{Figure 2.35 In an ac-coupled amplifier the dc resistance seen by the inverting terminal is } R_2; \]
  
  hence $R_i$ is chosen equal to $R_2$. 

  \[ \text{Figure 2.36 Illustrating the need for a continuous dc path for each of the op-amp input terminals. Specifically, note that the amplifier will not work without resistor } R_3. \]
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General Inverting Configuration

- 閉迴路轉移函數
  \[
  \frac{V_o(s)}{V_i(s)} = -\frac{Z_2(s)}{Z_1(s)}
  \]

Figure 2.37 The inverting configuration with general impedances in the feedback and the feed-in paths.
The Inverting Integrator

- A negative feedback for all frequencies except DC.
  
  $$i_i(t) = \frac{v_i(t)}{R}$$

  $$v_C(t) = v_C(0) + \frac{1}{C} \int_0^t i_i \, dt$$

  $$v_O(t) = -v_C(t) = -\frac{1}{CR} \int_0^t v_i(t) \, dt - v_C(0)$$

- RC is the time constant
- **Miller Integrator** is a LPF

---

Miller Integrator

- Integrator frequency
  
  $$\omega_{int} = \frac{1}{CR}$$

---

Figure 2.39 (a) The Miller or inverting integrator. (b) Frequency response of the integrator.
An integrator circuit with finite DC gain

\[ Z_1(s) = \frac{R_2}{1 + sR_2C_2} \]
\[ V_\alpha(s) = -I_2(s)Z_2(s) \]
\[ = -\frac{V(s)}{R_1}Z_2(s) \]
\[ T(s) = \frac{V_\alpha(s)}{V(s)} = \frac{-R_2 / R_1}{1 + sR_1C_2} \]

- DC gain: \[ T(\omega = 0) = -\frac{R_2}{R_1} \]
- Pole frequency: \[ \omega_p = \frac{1}{R_1C_2} \]

Figure 2.38 Circuit for Example 2.6.

Ex: 2.7

Figure 2.43 Waveforms for Example 2.7:
(a) Input pulse. (b) Output linear ramp of ideal integrator with time constant of 0.1 ms. (c) Output exponential ramp with resistor \( R_F \) connected across integrator capacitor.
The Differentiator

\[ i(t) = -C \frac{dv_t}{dt} \]
\[ v_o = -CR \frac{dv_t}{dt} \]
\[ T(s) = \frac{V_o(s)}{V_s(s)} = -sCR \]
\[ \frac{|V_o|}{|V_s|} = \omega CR \]
\[ \phi = -90^\circ \]

- Hi-frequency pole: \[ \omega_0 = 1/RC \]
- Differentiator is a HPF

Figure 2.44 (a) A differentiator. (b) Frequency response of a differentiator with a time-constant CR.